WHITEPAPER

MOBILE QUANTUM COMPUTING

The SaxonQ QC2026 Dual Core Quantum Computer

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Development and application of multi-core quantum computer based on NV technology for scalable, robust and mobile operation at room-temperature

SaxonQ

Where are we with Quantum Computing in 2026?

Quantum computing has reached a stage where multiple technological platforms coexist, each with distinct strengths and limitations. Today, leading approaches include superconducting qubits, trapped ions, neutral atoms, photonic systems, quantum dots, topological qubits, and solid-state spin defect systems such as nitrogen-vacancy (NV) centers in diamond.

Despite rapid progress, most of these platforms share a common constraint: they depend on highly controlled environments. Cryogenic cooling, ultra-high vacuum systems, vibration insulation and complex laser infrastructures are typically required to maintain quantum coherence and enable reliable operation.

These requirements impose significant limitations on system size, robustness, and deployability. In contrast, NV centers in diamond, offer a fundamentally different operational regime. They function at room temperature, do not require vacuum systems, and rely on comparatively simple optical and electronic control. This makes them uniquely suited for applications where quantum computing must move beyond laboratory conditions and into real-world environments. Mobile operation, industrial integration, and even future consumer products become feasible only under such conditions.

In addition, their compatibility with semiconductor-style fabrication processes opens a pathway toward scalable, cost-efficient production.

Key Challenges of Current Quantum Computers

Scaling: Qubit Count, Fidelity, and Architecture

A central challenge is increasing qubit count and gate fidelities toward quantum advantage and error correction thresholds for fault-tolerant quantum computing. At the same time, small noisy systems may already solve relevant problems if they are fast enough and supported by a large number of cores.

Accordingly, even leading players have shifted from scaling qubits per processor to improving fidelities and developing multi-core or multi-chip architectures. A key open issue remains the quantum mechanical connection of these cores. Current approaches rely on classical links and techniques such as circuit cutting, which introduce significant overhead and do not scale well for large, highly entangled problems. Multi-core systems are therefore best suited for applications with separable sub-problems, such as image recognition. Architectures enabling many identical cores with moderate qubit counts are particularly promising.

Speed and Time-to-Solution

Time-to-result is critical for industrial and consumer applications. Many relevant use cases, such as logistics, real-time image recognition, or energy grid stabilization, require decisions within seconds or milliseconds. Current quantum systems are typically not designed for such time-critical scenarios. Progress requires not only higher qubit counts, but also faster computation, readout, and parallelization.

System Scaling and Hardware Overhead

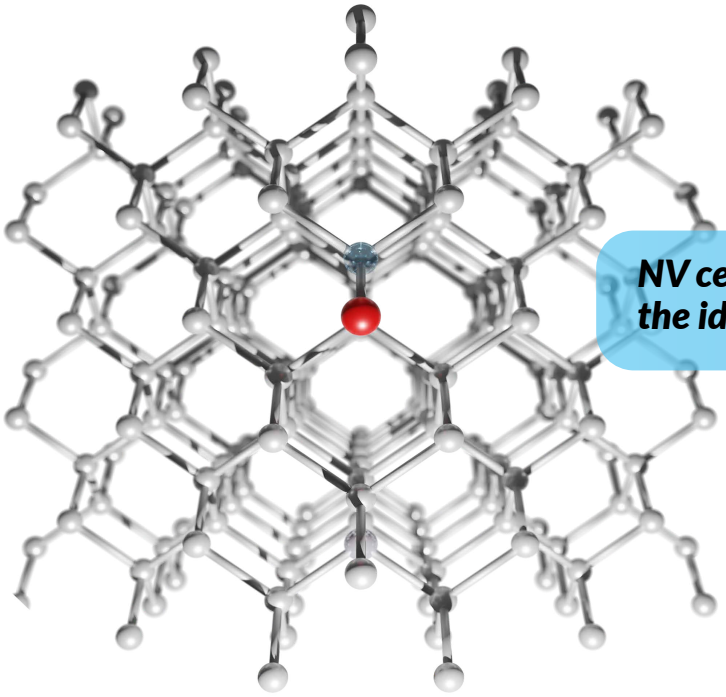
Scaling quantum systems leads to rapidly increasing hardware complexity. Many platforms require multiple control lines per qubit, as well as growing cryogenic, vacuum, and laser infrastructure. This limits scalability, restricts parallelization, and poses unresolved challenges for control electronics at larger system sizes.

Energy Consumption

Energy efficiency is becoming a key factor, particularly with rising computational demand from AI. Quantum advantage may already be relevant if energy cost per calculation is lower than for classical systems. Infrastructure-heavy approaches are inherently limited in this regard.

Cost and Deployability

High system and operational costs, as well as infrastructure requirements, remain major barriers. Systems relying on cryogenics and complex machinery are difficult to deploy in industrial environments, mobile systems, or consumer applications, where space, cost, and robustness are critical.



Overcome Challenges with NV Technology

NV centers in diamond as atomic-scale defects are the ideal room temperature multi-core platform.

NV centers are atomic scale

NV centers are atomic-scale modifications of the diamond crystal lattice where a nitrogen atom replaces a carbon atom, and an adjacent vacancy (missing carbon atom) is present in the lattice. These so-called “color centers“ have remarkable capabilities that are highly suited as quantum bits (qubits) for quantum computing.

NV centers are highly reliable spin qubits

A key benefit of NV centers is their reliability as spin qubits. Spins are fundamental quantum mechanical constituents that define the qubits. For NV quantum computing, the NV centers must be negatively charged. SaxonQ’s patented co-doping technique, using sulfur atoms as donors, ensures that the NV centers remain negatively charged, **maintaining stable and reliable qubit operation [1]**.

NV centers are highly scalable – with multicore technology and NV arrays

By combining arrays of NV centers with nuclear spin qubits, SaxonQ’s quantum processing units (QPUs) can efficiently scale to multi-core systems. This is facilitated by SaxonQ‘s ion implantation technology allowing a large number of identical quantum cores to be fabricated in short time on a single diamond chip — a possibility fundamentally denied to other qubit technologies.

Thanks to their simplicity, small size, and cost-effective setup, these QPUs can be operated together in parallel for faster processing, **enhancing the computational power** of quantum algorithms.

SaxonQ‘s advanced ion implantation technology allows to go beyond single NV centers, enabling the creation of dense arrays of NV centers. Within these arrays, quantum information is exchanged through dipole-dipole interactions, forming larger quantum registers capable of more complex computations. The beginning of this scaling has started with NV-NV pairs and will continue to linear and 2D arrays.

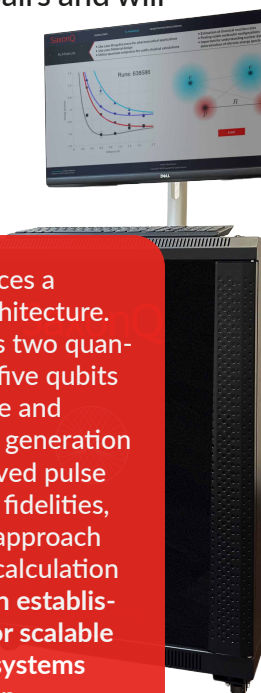
Evolution of the SaxonQ System

The SaxonQ quantum computer evolved from a sensitive laboratory setup into a deployable product through continuous system integration and miniaturization.

Generation 1 marked the transition from prototype to CE-certified system, with automated startup and self-calibration enabling operation without specialized expertise.

Generation 2 focused on usability and integration. The system was significantly reduced in size, suitable for office environments, and combined with the full-stack software suite Gemstone®, allowing users to submit jobs without managing hardware complexity.

Generation 3 introduces a mobile multi-core architecture. The system integrates two quantum chips with up to five qubits each, fully controllable and operated via the next generation of Gemstone®. Improved pulse design increases gate fidelities, while a new readout approach significantly reduces calculation times. **This generation establishes the foundation for scalable multi-core quantum systems with parallel operation.**



Advantages and Challenges of NV-Center-Based Systems

NV-center-based quantum computers enable operation at room temperature without cryogenics, vacuum systems, or complex laser infrastructure. The qubits are inherently stable within the diamond lattice, allowing for compact, robust, and mobile systems. Combined with automated calibration and intuitive software, operation requires no specialized expertise.

Their chip-based architecture allows scalable multi-core designs without significant infrastructure overhead. Systems remain compact and energy-efficient, operating at only a few hundred watts, with further reductions expected.

In addition, the physical structure of NV centers enables native multi-qubit operations within a single node, reducing circuit complexity. At the same time, scaling qubit numbers per core remains challenging. Strong coupling between NV centers requires nanometer-scale placement precision, making deterministic implantation and high creation yield critical. Additional challenges include minimizing cross-talk, scaling control electronics, and enabling precise, position-resolved readout.

In all of these areas, SaxonQ is advancing key technologies toward scalable, application-ready systems.

Third Generation SaxonQ Quantum Computer

The third-generation SaxonQ system introduces a dual-core QPU, enabling true multi-core operation, parallel job execution, and simultaneous processing. The system fully operates at room temperature in standard office environments. Both quantum cores have been optimized for coherence times, gate fidelities, and computation speed. Control is refined at the pulse level, including gate operations, phase control, initialization, and readout, supported by improved control hardware.

A redesigned readout architecture, combining advanced optical elements and an enhanced signal-to-noise ratio for quantum measurements, significantly accelerates computation.

In parallel, the underlying diamond material and fabrication processes have been optimized to improve qubit quality and stability as well as control pulse delivery further increasing coherence times.

QC 2026 DUAL CORE

SPECIFICATION	Gen 1	Gen 3	Simulated for Gen 3
Warm-up time	4 h	< 1 h	
Qubit cores	1	2 (seperately with different jobs or as one parallel system)	2
Qubits per core	4	4 or 5	up to 5
One-Qubit gate fidelity	0.95	up to 0.9992	> 0.999
Two-Qubit gate fidelity	0.92	0.97	> 0.99
Computational speed relative to Gen 1	1	> 10	
Power consumption	600 W	600 W	
API and interfacing	Script-based user interface remote control supported	Graphical user interface API/cloud access fully enabled by Gemstone® Integrated job queue and job database	
Quantum circuits	OpenQASM/Qiskit support Transpilation and execution of user defined quantum circuits	OpenQASM/Qiskit support / Transpilation and execution of user defined quantum circuits / Graphical quantum circuit builder/ Graphical job inspector with real-time result evaluation	

Comparison of specifications for the SaxonQ Gen3 quantum computer compared to the Gen1 system, simulated results.

A key feature of the system is that core components of the control electronics do not need to be duplicated. As a result, the system remains compact and energy-efficient while reducing cost per quantum core - an important step toward scalable, consumer-ready quantum computing.

The third-generation system demonstrates independent control of two NV-center-based cores, enabling parallel execution of tasks and multiple jobs. Its architecture is inherently multi-core ready, allowing straightforward scaling to virtually unlimited core counts.
This scalability was demonstrated at the Hannover Messe 2026, where two physical cores were operated alongside several simulated quantum cores. The system is upgradeable, enabling additional cores to be added to existing installations at significantly lower cost than deploying new systems.

This architecture enables near-linear speedup for applications that can be decomposed into independent tasks and establishes the foundation for scalable, multi-core quantum computing systems.

Moreover, the user is free to add an **almost unlimited amount of simulated quantum cores** with freely selectable qubit parameters. Alternatively, this allows a fully simulated multi-core systems as digital twin for testing of quantum circuits, educational resource and/or comparison with the behaviour of the physical cores.

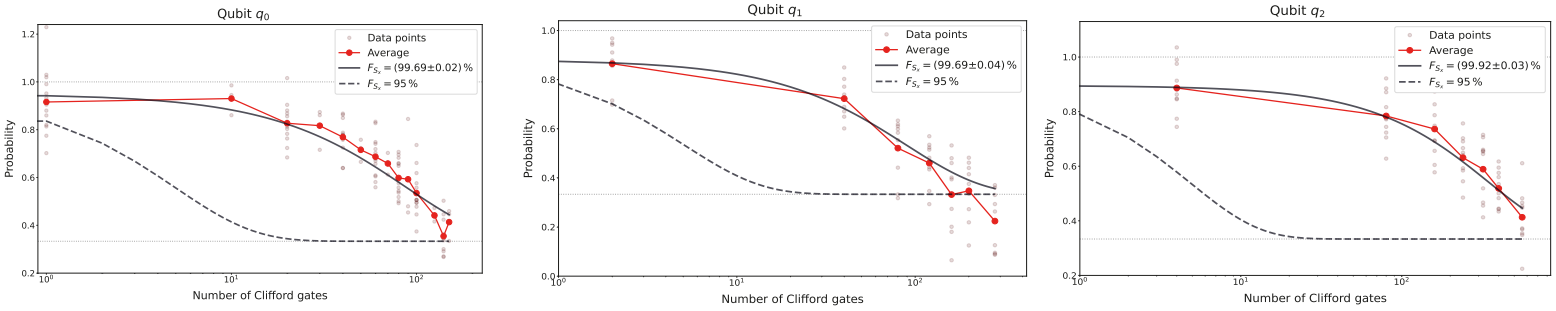
Qubits per core

Quantum chips with fully entangled qubits

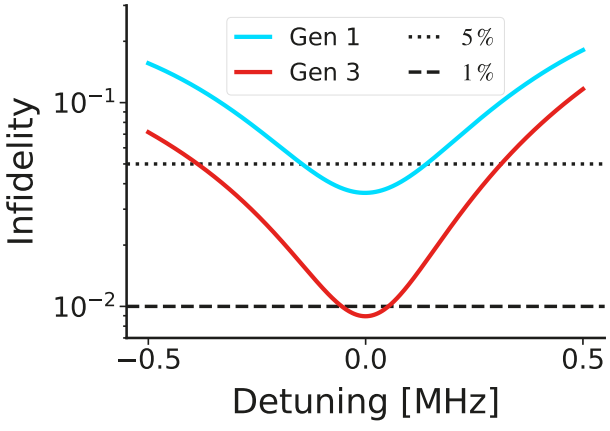
Number of quantum processors (multicore)

For parallel and distributed execution of quantum algorithms

Possible configurations of a quantum processor with fully entangled qubits on parallel chips



Determination of one-qubit gate fidelities for the nuclear spin qubits of a Gen3 system by randomized benchmarking. Dashed lines correspond to curves expected for the gate fidelities of the Gen1 system.



Simulated pulse parameter optimization for our multi-qubit gates towards maximized fidelities. The orange curve are correspond to the Gen1 pulses, while the blue curve represents the optimized pulses for the Gen3 sytem.

The minimal value of the infidelity of <0.01 implies a gate fidelity of >0.99 for the multi-qubit gate for our optimized gate pulses.

Possible Use Cases

Multi-core QPUs enable the execution of larger quantum algorithms by distributing them across several smaller cores. This can be achieved via circuit cutting, where a problem is divided into sub-circuits that run on individual cores, with classical dependencies between cores and results recombined afterward. However, this approach introduces significant classical computation overhead and does not scale well for highly entangled problems [2]. **The strongest use cases therefore lie in problems that can be naturally decomposed into independent or weakly coupled sub-tasks**, where parallel execution leads to efficient scaling.

Image Recognition and Image Classification

Images can be decomposed into independent regions and processed in parallel across multiple QPU cores. Each core extracts relevant features, which are then combined to form a final decision. This approach can be further extended using circuit-cutting techniques where applicable.

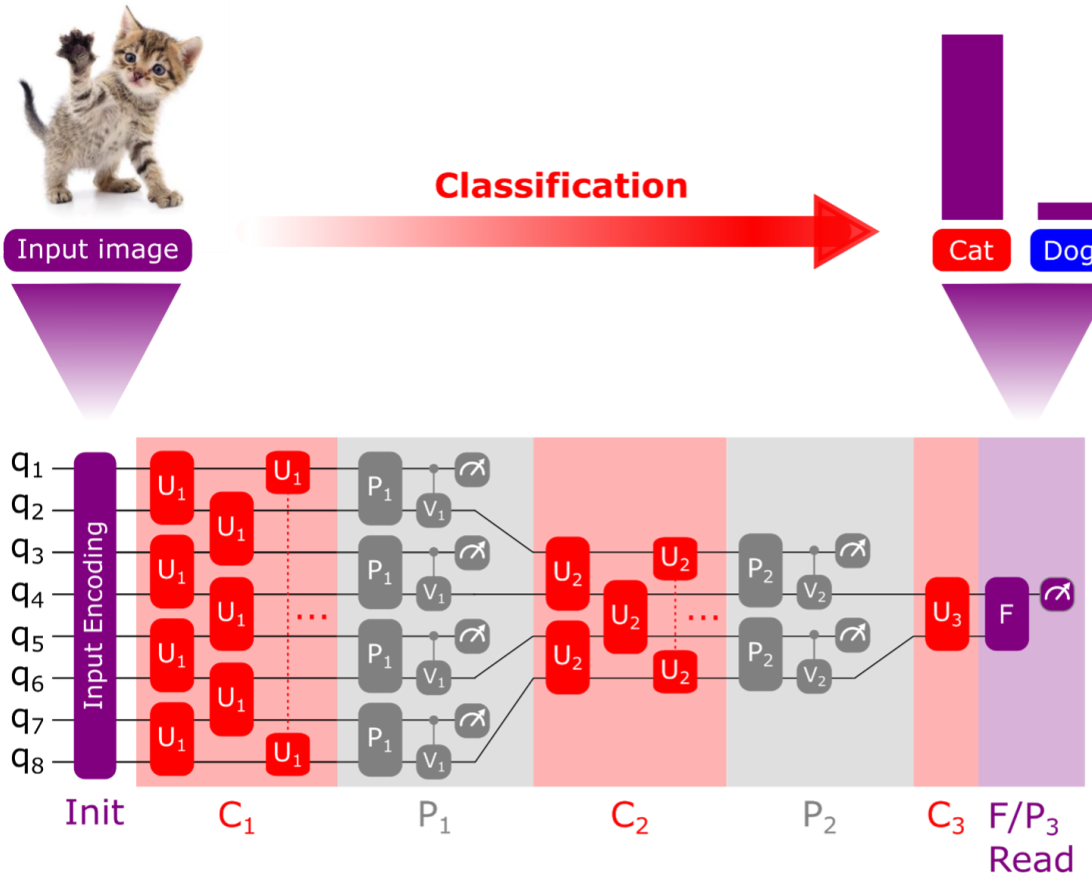
Quantum Machine Learning and Quantum Neural Networks

Hybrid quantum-classical models have shown advantages over purely classical approaches, even on small quantum processors with only a few qubits [3]. This opens the door to practical applications in machine learning and AI already at low qubit counts.

Multi-core quantum systems enable parallel execution of such models, significantly accelerating both training and inference. NV-center-based architectures are particularly well suited for this, as they allow the implementation of many parallel cores within a single system.

In the context of rapidly growing AI workloads, energy efficiency becomes a critical factor. If hybrid quantum-classical approaches reduce the energy cost per operation compared to classical tensor processors, this could provide a meaningful quantum advantage, not only in performance, but also in sustainability.

Potential applications include real-time decision-making in automotive, industrial, and medical contexts, where classification of an input is sufficient:



Sketch of the principle of quantum convolution neural networks for image classification.

The input image is fed into the quantum circuit and after several convolution (C) and pooling layers (P), a binary classification result is obtained (cat or dog) after qubit readout following the preparation of the fully connected layer (F).

Adapted from [5]. Stock image of cat from www.shutterstock.com # 70175115.

Is there a need to stop the car or not?
Does a component need to be sorted out or not?
Does the patient have cancer or not?
Does the patient need surgery or not?

Quantum Machine Learning

Quantum information processing may prove crucial for reducing the energy consumption of artifical intelligence. SaxonQ's mobile quantum processors with a low-energy footprint will facilitate image recognition, a key component of autonomous driving, in particular.

An image classification example run on a SaxonQ mobile QPU, where the quantum system classifies an image as being a smiley or not.

These scenarios require decisions within fractions of a second. Parallel execution on multi-core QPUs, combined with fast readout, provides a pathway toward meeting these real-time requirements.

In particular, in medical imaging, AI-based classification already shows performance comparable to human experts, e.g. in [4] while significantly reducing evaluation time, highlighting the potential for quantum-enhanced systems to further support such applications.

Quantum convolutional neural networks (QCNNs) can already run on small quantum cores and enable fast, energy-efficient image classification [5]. Similarly, in natural language processing, quantum mixed-state self-attention networks can operate on single-digit qubit systems [6].

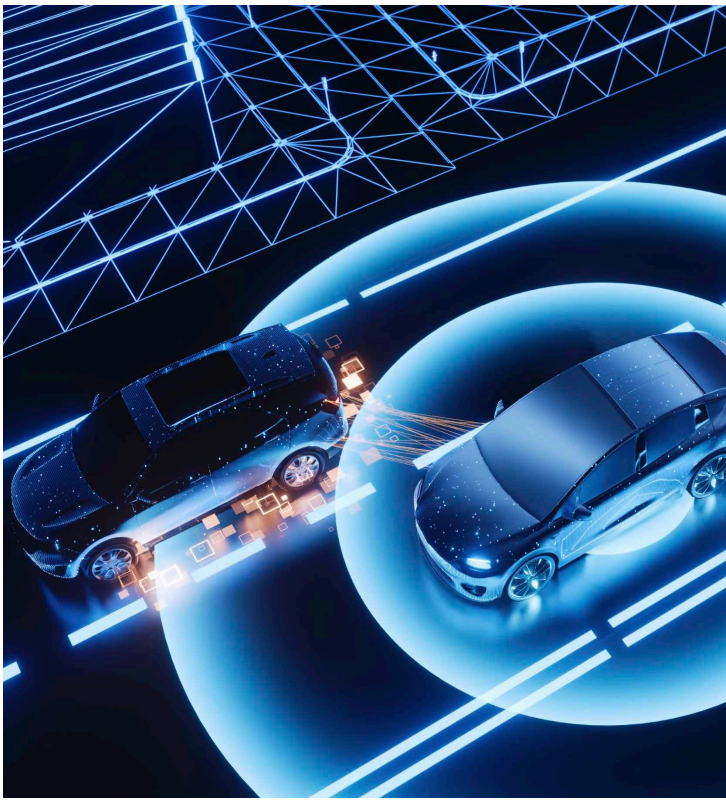
The practical feasibility of such approaches has been demonstrated on our QPUs, for example by live classification of whether a drawn image represents a smiley using a single qubit.

Optimization for the finance sector or distribution of energy

Optimization problems such as portfolio management in finance or energy distribution in power grids can benefit from multi-core quantum systems. Using techniques like circuit cutting, larger optimization tasks can be distributed across multiple QPUs. Proof-of-principle studies have already demonstrated competitive results for real-world portfolio optimization [7].

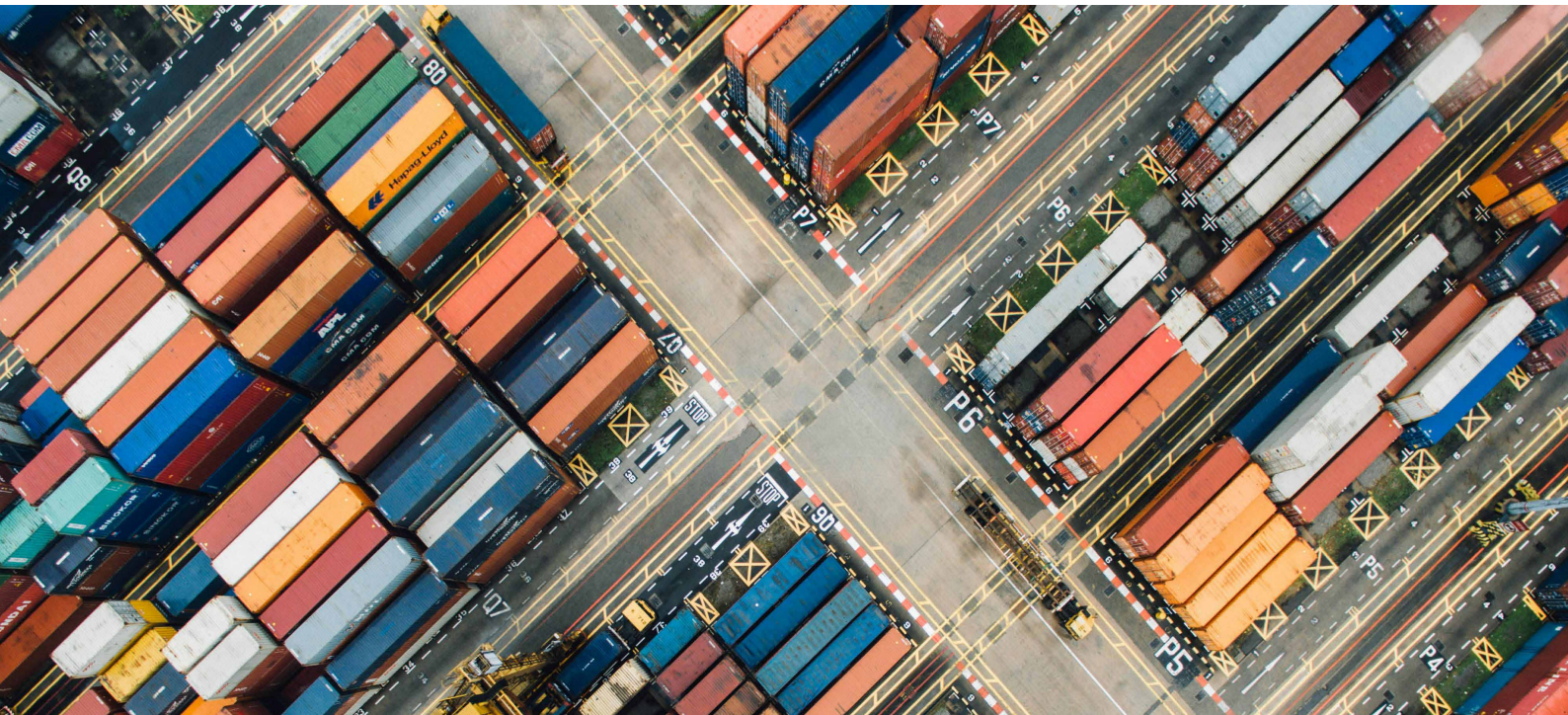
Beyond optimization, multi-core architectures enable true parallel access to quantum hardware. This is particularly relevant for educational and research environments, where multiple users require hands-on interaction with quantum systems.

Instead of relying on multiple machines or costly cloud access, several users can run experiments simultaneously on different cores of a single system. The integrated Gemstone® software supports this through built-in job queuing and network integration. This concept was demonstrated in a live multi-core setup at the Hannover Messe 2026.



Finally, identical quantum cores can be used to execute the same computation in parallel, significantly reducing runtime. Since quantum results rely on repeated measurements (shot statistics), parallel execution allows faster accumulation of results, leading to near-linear speedup with the number of cores.

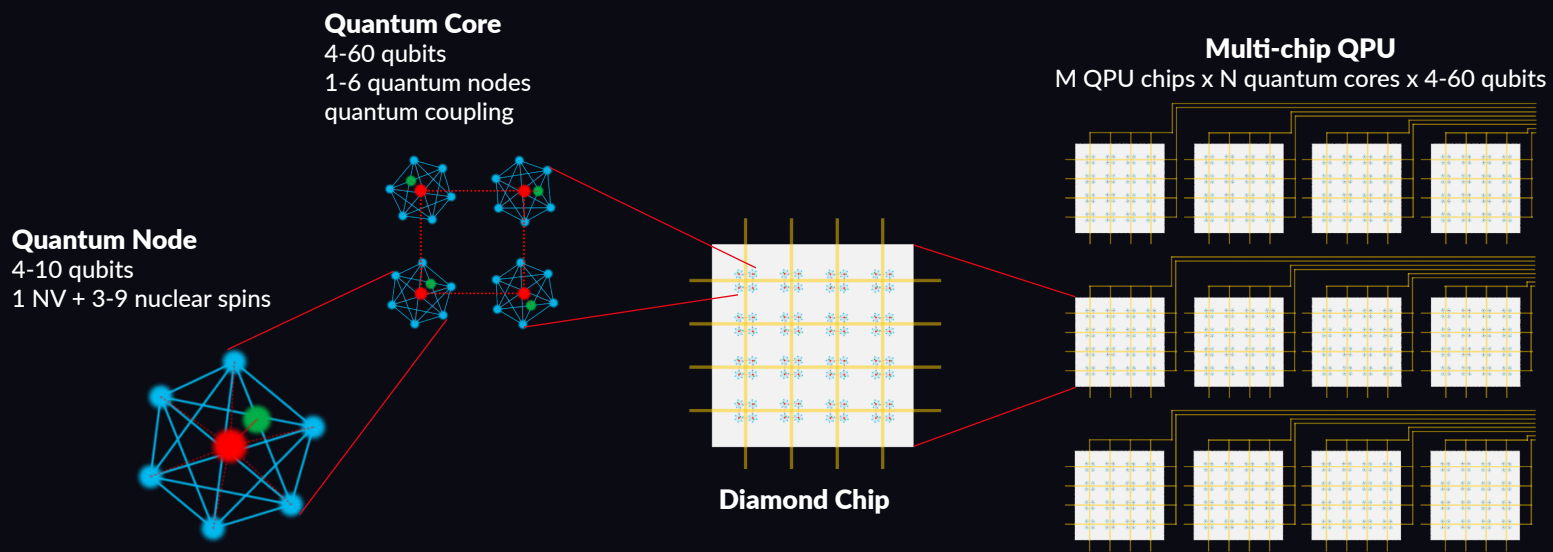
This is particularly relevant for time-critical applications such as real-time decision-making in logistics, energy systems, or autonomous driving.



Outlook and Scaling

The next steps focus on two parallel scaling paths: increasing the number of qubits per core and expanding the number of cores per system. This includes advancing implantation techniques to realize arrays of coupled NV centers, as well as improving control methods to access larger nuclear spin registers per center, potentially exceeding ten qubits per node.

By coupling these registers and integrating multiple cores and chips within a single system, multi-chip, multi-core QPUs with significantly increased qubit counts can be realized while maintaining a unified control architecture.



Sketch of the upscaling approach employing multiple quantum chips as realized by the third generation SaxonQ quantum computer in combination with multiple quantum cores per chip.

Further improvements will focus on enhancing qubit quality through optimized diamond material, NV-center creation, and chip processing, aiming to further increase fidelities and coherence times.

In parallel, SaxonQ is driving miniaturization toward industry-ready systems. Advanced electrical readout methods will reduce system size while increasing readout speed and overall computational performance — key for time-critical applications such as automotive use cases. **Future developments include custom, miniaturized control electronics and on-chip architectures to further shrink system footprints.**

	2023	2025	2026	2027	2030
# of NV	1	2	3	4	>8
# of nuclei per NV	3	5	9	10	>10
qubits per core	4	12	30	>40	>80
# of cores	1	2	4	32	128
total # of qubits	4	24	120	>1.000	>10.000

"We have taken another step toward miniaturizing multi-core quantum systems, bringing the quantum computer closer to a chip-scale reality."

Prof Marius Grundmann

Source References

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